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EXAMINER	
TRAN, TAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,134	SHIMIZUME, KAZUTOSHI	
	Examiner	Art Unit	
	TAN N TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 11/04/03* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2 and 3* is/are allowed.

6)☒ Claim(s) *1,4,5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. If applicant is aware of any relevant prior art, he/she requested to cite it on form PTO-1449 in accordance with the guidelines set forth in M.P.E.P. **609.**

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1,4 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not disclose each of said plurality of mounted logic circuits is operated by setting a SEL signal for selectively turning a plurality of transistor on and off as recited in claim 1.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 9-11, "each of said plurality of mounted logic circuits is operated by setting a SEL signal for selectively turning a plurality of transistor on and off" is unclear as to whether it is being referred to each of said plurality of mounted logic circuits is operated by setting a SEL signal for selectively turning a plurality of transistor on or off.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,4,5 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (6,446,249) in view of Gilliam (5,566,107).

With regard to claim 1, Wang et al. discloses an I/O region formed on a chip 425 and having at least an input/output pad 435; a plurality of active region 505 formed on the chip 425; the active region 505 being separated from one another by a boundary spacer; a plurality of logic circuits having either one of the same functions and different functions being mounted in each of

the active regions 505, and a selection circuit (Note fig. 14) for selectively operating only one of the plurality of mounted logic circuits. (Note figs. 1B, 10,11,14 of Wang et al.).

Wang et al. does not disclose each of plurality of mounted logic circuit is operated by setting an SEL signal for turning on/off a transistor for each of the mounted logic circuit to one of a high and a low level.

However, Gilliam discloses a selection circuit 26 for selectively operating only one of the plurality of mounted logic circuit 18; each of the plurality of mounted logic circuit 18 is operated by setting an SEL signal for turning on/off a transistor 82(84) for each of the mounted logic circuit 18 to one of a high and a low level. (Note figs. 1,3 of Gilliam).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Wang et al.'s device having the logic circuit is operated by setting an SEL signal for turning on/off a transistor for each of the mounted logic circuit to one of a high and a low level such as taught by Gilliam for enabling an associated function circuit in response to an activate signal.

With regard to claims 4,5, Wang et al. discloses an I/O region formed on a chip 425 and having at least an input/output pad 435; a plurality of active region 505 formed on the chip 425; the active region 505 being separated from one another by a boundary spacer; a plurality of logic circuits having either one of the same functions and different functions being mounted in each of the active regions 505, and a selection circuit (Note fig. 14) for selectively operating only one of the plurality of mounted logic circuits. (Note figs. 1B, 10,11,14 of Wang et al.).

Wang et al. does not disclose the selection circuit includes a transistor element connected in series with each the logic circuit between the logic circuit and a power terminal; the selection

circuit or transistor element selects a logic circuit to be operated on a basis of a signal input supplied from an outside through the input/output pad.

However, Gilliam discloses the selection circuit 26 includes a transistor element 60 connected in series with the logic circuit 72 between the logic circuit 72 and a power terminal Vcc, the selection circuit or transistor element selects a logic circuit to be operated on a basis of a signal input supplied from an outside through activate signal serves as the input/output pad. (Note fig. 3 of Gilliam).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Wang et al.'s device having the selection circuit includes a transistor element connected in series with each the logic circuit between the logic circuit and a power terminal, the selection circuit or transistor element selects a logic circuit to be operated on a basis of a signal input supplied from an outside through activate signal serves as the input/output pad such as taught by Gilliam in order to enabling an associated function circuit in response to an activate signal.

Allowable Subject Matter

4. Claims 2,3 are allowable over the prior art of record because none of these references disclose or can be combined to yield the claimed invention such as the buffer circuit being substantially free of transistors and inverters as recited in claim 2.

Response to Arguments

5. Applicant's arguments filed 11/04/03 have been fully considered but they are not persuasive.

It is argued, at page 6 of the remarks, that "Neither Wang, Gilliam, or any combination thereof discloses or suggest selectively operating only one of a plurality of mounted logic circuits, or a plurality of mounted logic circuits operated by setting an SEL signal for selectively turning a plurality of transistors on and off for each of the mounted logic circuits of one of a high and a low level". However, figs. 1,3 of Gilliam does show a selection circuit 26 for selectively operating only one of the plurality of mounted logic circuit 18; each of the plurality of mounted logic circuit 18 is operated by setting an SEL signal for turning on/off a transistor 82(84) for each of the mounted logic circuit 18 to one of a high and a low level. Therefore, it would have been obvious to one of ordinary skill in the art to form the Wang et al.'s device having the logic circuit is operated by setting an SEL signal for turning on/off a transistor for each of the mounted logic circuit to one of a high and a low level such as taught by Gilliam in order to enabling an associated function circuit in response to an activate signal.

It is argued, at page 7 of the remarks, that "Neither Wang, Gilliam, nor any combination thereof discloses or suggests a selection circuit for selectively operating only one of said plurality of mounted logic circuits, wherein said selection circuit includes a transistor element connected in series with each said logic circuit between said logic circuit and a power terminal, said transistor element selects a logic circuit to be operated on a basis of a signal input supplied through said input/output pad". However, fig. 14 of Wang et al. does show a selection circuit for selectively operating only one of the plurality of mounted logic circuits and fig. 3 of Gilliam does show the selection circuit 26 includes a transistor element 60 connected in series with the logic circuit 72 between the logic circuit 72 and a power terminal Vcc, the selection circuit or transistor element selects a logic circuit to be operated on a basis of a signal input supplied from

an outside through activate signal serves as the input/output pad. Therefore, it would have been obvious to one of ordinary skill in the art to form the Wang et al.'s device having the selection circuit includes a transistor element connected in series with each the logic circuit between the logic circuit and a power terminal, the selection circuit or transistor element selects a logic circuit to be operated on a basis of a signal input supplied from an outside through activate signal serves as the input/output pad such as taught by Gilliam in order to enabling an associated function circuit in response to an activate signal. Thus, applicant's claims 1,4,5 do not distinguish over Gilliam and Wang et al. references.

Conclusion

7. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

Dec 2003

Minhloan Tran
Primary Examiner
Art Unit 2826